

Homework 5

Due: Nothing to turnin, for Quiz review only.

Turnin: Nothing.

1. — (Problem 5.17 [5] <§5.5>, see the Chapter 5 exercises on the CD) This exercise is similar to Exercise 5.15, but this time consider the effect that the stuck-at-0 faults would have on the multiplexors in the multiple-cycle datapath in Figure 5.28 on page 323 (and slide 25 of 5-Processor: Datapath and Control from the lecture notes). Consider each of the following faults: $\text{RegDst} = 0$, $\text{MemtoReg} = 0$, $\text{IorD} = 0$, $\text{ALUSrcA} = 0$.

2. — (Problem 5.18 [5] <§5.5>, see the Chapter 5 exercises on the CD) This exercise is similar to Exercise 5.17, but this time consider stuck-at-1 faults (the signal is always 1).

3. — (partial) (Problem 5.29 [5] <§5.5> page 356) This exercise is similar to Exercise 5.2, but this time consider the effect that the stuck-at-0 faults would have on the multiple-cycle datapath in Figure 5.27, page 322 (and slide 25 of 5-Processor: Datapath and Control from the lecture notes). Consider each of the following faults:

- a. $\text{RegWrite} = 0$
- b. $\text{MemRead} = 0$
- c. $\text{MemWrite} = 0$
- d. $\text{IRWrite} = 0$
- e. $\text{PCWrite} = 0$
- f. $\text{PCWriteCond} = 0$

For parts e. and f., refer to slides 33 through 35 of the 5-Processor: Datapath and Control from the lecture notes.

4. — (partial) (Problem 5.30 [5] <§5.5> page 356) This exercise is similar to Exercise 5.29, but this time consider stuck-at-1 faults (the signal is always 1).

- a. $\text{RegWrite} = 1$
- b. $\text{MemRead} = 1$
- c. $\text{MemWrite} = 1$
- d. $\text{IRWrite} = 1$
- e. $\text{PCWrite} = 1$
- f. $\text{PCWriteCond} = 1$

For parts e. and f., refer to slides 33 through 35 of the 5-Processor: Datapath and Control from the lecture notes.