Position: Fabric Performance Architect

The Data Center Group drives new products technologies from high-end co-processors for supercomputers to low-energy systems for the cloud, as well as solutions for big data and intelligent devices. The group is a worldwide organization that develops the products and technologies that power nine of every 10 servers sold worldwide.

Intel's Technical Computing Group is defining a new interconnect/fabric architecture for large scale, high performance HPC and Big Data systems. To support architecture exploration and performance validation of such systems, we are developing a state-of-the-art simulation methodology. We are looking for a senior engineer / architect to work on significant aspects of the new methodology including: 1) development of new NIC and switch performance models, 2) optimizations to improve simulation speed, 3) the ability to simulate realistic workloads and 4) new visualization capabilities for efficient analysis. We expect the candidate to develop new simulation capabilities and also effectively use the capabilities to analyze architecture trade-offs. This is a new project with opportunities to have a significant impact on the interconnect architecture and system level features.

Minimum Qualifications:

MS or PhD with 2-4 years of experience. New PhD grad will be considered if their academic background matches required skills.

- 2+ years of experience showing proficiency in C and C++ programming
- 2+ years of experience with computer architecture including knowledge of cache coherency, I/O and memory subsystems

Additional Preferred Qualifications:

- Performance modeling experience
- Logic design and RTL development experience
- Familiarity with HPC or Big Data applications