- Attackers: need to analyze our program to modify it!
- Defenders: need to analyze our program to protect it!
- Two kinds of analyses:
  - static analysis tools collect information about a program by studying its code;
  - *dynamic analysis tools* collect information from executing the program.

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- decompilation: turn raw assembly code into source code.

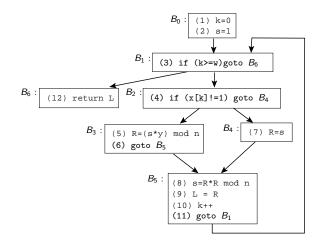
#### Outline



# Control-flow Graphs (CFGs)

- A way to represent functions.
- Nodes are called basic blocks.
- Each block consists of straight-line code ending (possibly) in a branch.
- An edge  $A \rightarrow B$ : control could flow from A to B.

#### The resulting graph



Static Analysis

#### BUILDCFG(F):

- Mark every instruction which can start a basic block as a *leader*:
  - the first instruction is a leader;
  - any target of a branch is a leader;
  - the instruction following a conditional branch is a leader.
- A basic block consists of the instructions from a leader up to, but not including, the next leader.
- ③ Add an edge  $A \rightarrow B$  if A ends with a branch to B or can fall through to B. □

#### Interprocedural control flow

- *Interprocedural analysis* also considers flow of information between functions.
- Call graphs are a way to represent possible function calls.
- Each node represents a function.
- An edge  $A \rightarrow B$ : A might call B.

### Building call-graphs

```
void h();
      void f(){
          h();
      void g(){
          f();
                                         k
      void h() {
                                 main
                                                          g
        f();
        g();
      }
Static Analysy Oid
            k() {}
```

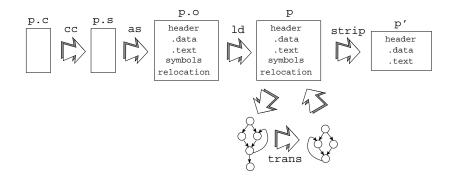
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#### Outline

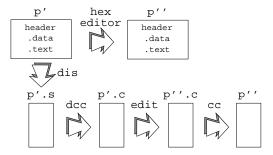


Disassembly

#### Reconstituting source



### Attacking stripped binary code



• Variable length instruction sets — overlapping instructions.

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- Self-modifying code.

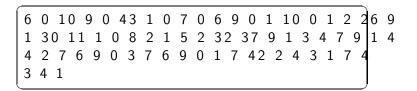
opcode	mnemonic	operands	semantics
0	call	addr	function call to addr
1	calli	reg	function call to address in reg
2	brg	offset	branch to $\mathrm{pc}\!+\!\mathit{offset}$ if flags for
			> are set
3	inc	reg	$\textit{reg} \leftarrow \textit{reg} + 1$
4	bra	offset	branch to $\mathrm{pc}+\mathit{offset}$
5	jmpi	reg	jump to address in <i>reg</i>
6	prologue		beginning of function
7	ret		return from function

- Instruction set for a small architecture.
- All operators and operands are one byte long.
- Instructions can be 1-3 bytes long.

Reconstituting source

opcode	mnemonic	operands	semantics
8	load	$reg_1, (reg_2)$	$reg_1 \leftarrow [reg_2]$
9	loadi	reg, imm	$\textit{reg} \leftarrow \textit{imm}$
10	cmpi	reg, imm	compare <i>reg</i> and <i>imm</i> and set
			flags
11	add	$reg_1, reg_2$	$\mathit{reg}_1 \gets \mathit{reg}_1 + \mathit{reg}_2$
12	brge	offset	branch to $\mathrm{pc}+\textit{offset}$ if flags for
			$\geq$ are set
13	breq	offset	branch to $\mathrm{pc}+\textit{offset}$ if flags for
			= are set
14	store	$(reg_1), reg_2$	$[\mathit{reg}_1] \gets \mathit{reg}_2$

#### Disassembly — example



- Next few slides show the results of different disassembly algorithms.
- Correctly disassembled regions are in pink.

Í	main: # ORIC	GINAL PROG	RAM	ľ			
	0: [6]	prologue					
l	1: [0,10]	call	foo				
l	3: [9,0,43]	loadi	r0,4	ļ	<sup>8</sup> bar:		
l	6: [1,0]	calli	r 0		Dar. 12.[6]	nrologuo	
	8: [7]	ret			43:[6]		
l	9: [0]	.align	2		44:[9,0,3]		r0,3
l	foo:				47:[7]	ret	
l	10:[6]	prologue			baz:		
l	11:[9,0,1]	loadi	r0,1		48:[6]		
l	14:[10,0,1	cmpi	r0,1		49:[9,0,1]		r0,1
	17:[2,26]	brg	26		52:[7] _life:	ret	
	19:[9,1,30]	loadi	r1,3	3		ht.a	40
l	22:[11,1,0]	add	r1 ,	r	53:[42] fred :	.byte	42
l	25:[8,2,1]	load r2,(	r1)			h	л
l	28:[5,2]	jmpi	r2		54:[2,4]	brg	4 #1
l	30:[32]		32		56:[3,1]		r1
l	31:[37]		37		58:[7]	ret	2
	32:[9,1,3]		r1,3	8	59:[4,3]	bra	3
	35:[4,7]	bra	7		61:[4,1]	bra	1

# LINEAR SW	EEP DISASS	EMBI	Įγ	/		
0: [6]	prologue					
1: [0,10]	call	10				
3: [9,0,43]	loadi	r0,4	3			
6: [1,0]	calli	r0	ſ	43:[6]	prologue	
8: [7]	ret				prologue	-0 1
9: [0,6]	call	6		44:[9,0,3]		r0, <b>3</b>
11:[9,0,1]	loadi	r0,1		47:[7]	ret	
14:[10,0,1]	cmpi	r0,1		48:[6]		
17:[2,26]		26		49:[9,0,1]		r0,1
19:[9,1,30]	loadi	r1,3	KI I I	52:[7]	ret	40
22:[11,1,0]	add	r1 ,		53:[42]	ILLEGAL	42
25:[8,2,1]				54:[2,4]	brg	4
28:[5,2]		•		56:[3,1]		r1
30:[32]		32		58:[7]	ret	0
31:[37]		37		59:[4,3]	bra	3
32:[9,1,3]		r1,3	3	61:[4,1]	bra	1
	bra	7				
37:[9,1,4]	loadi	r1,4	1			
40:[4,2]	bra	2				

			32:[9,1,3]	loadi	r1,3
f0: # RECUR		ERSA	35:[4,7]	bra	7
0: [6]			37:[9,1,4]		r1,4
1: [0,10]		10		bra	2
3: [9,0,43]	loadi	r0,4	42:[7]	ret	2
6: [1,0]	calli	r0			
8: [7]	ret		43:[6]	prologue	
			44:[9,0,3]		r0,3
9: [0]	. byte	0	47:[7]	ret	
	-				c
f10:			48:[6]	byte	6
10:[6]	prologue		49:[9]	byte	9
11:[9,0,1]		r0,1	50:[0]	byte	0
14:[10,0,1]		r0,1	51:[1]	. byte	1
17:[2,26]	brg	26	52:[7]	.byte	7
19:[9,1,30]	-	r1,3	53:[42]	. byte	42
22:[11,1,0]	add	r1,	54:[2]	. byte	2
25:[8,2,1]					
28:[5,2]		r2	59:[4]	.byte	4
	jmpi hvto		60:[3]	. byte	3
30:[32]	byte	32	61:[4]	.byte	4

• Extends the standard recursive traversal algorithm with a collection of heuristics to inrease precision.

## Algorithm REHM

- Extends the standard recursive traversal algorithm with a collection of heuristics to inrease precision.
- First, follow all branches and returns a set of function start addresses and a set of decoded addresses.

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- Next, try to build a reasonable control flow graph from the remaining undecoded bytes.
- Reasonable CFG: "there are no jumps into the middle of another instruction and the resulting function contains at least two control transfer instruction."

f0: # HARRIS/	MILLER				
0: [6]	prologue		f43 :		
1: [0,10]	call	10	43:[6]	nrol	ogue
3: [9,0,43]	loadi	r0	44:[9,0		di r0,3
6: [1,0]	calli	r 0	47:[7]	ret	
8: [7]	ret		+ / . [ / ]	Tet	
9: [0]	. byte	0	f48:		
(1.0			48:[6]	pro	ogue
f10:			49:[9,0		di r0
10:[6]	prologue	-	52:[7]	ret	
11:[9,0,1]	loadi	r0			
14:[10,0,1]	cmpi	r0	53:[42]	. by	te 42
17:[2,26]		26			
19:[9,1,30]	loadi	r1	B0 f54.		
22:[11,1,0]	add	r1	54:[2,4]	brg	4
25:[8,2,1]	load r2	,(r1	56:[2,4]		r1
28:[5,2]	jmpi	r 2	58:[7]	ret	11
30:[32]	. byte	32	50.[7]	ret	
31:[37]	. byte	37	F 0 . [ 4 ]	had	
32:[9,1,3]	loadi	r1	359:[4]	. by	te 4

 Function f43 is only called indirectly, function f48 isn't called at all — the disassembler still finds them by searching for their prologue instructions.

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- The disassembler next starts at location 53, realizes that 42 isn't a valid opcode, moves to location 54, builds a valid CFG.
- The algorithm recovered 95.6% of all functions over a set of Windows and Linux programs.