Mohan Rajagopalan

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Senior Research Scientist / Staff Software Engineer,
Microprocessor and Programming Research
Intel Labs; Santa Clara, CA-95054

RESEARCH INTERESTS

Prototyping, developing, and optimizing systems. Adapting exploratory research to bring new technology to market.
Operating Systems : Scheduling, and quality of service for multi-core systems
Systems Design : Adaptive models for computation, scalability, reliability, and security
Compilers : Static and dynamic optimization, language design, and binary rewriting

EDUCATION

Ph.D in Computer Science **Jan 2006**
University of Arizona
Thesis : *Optimizing System Performance and Dependability using Compiler Techniques*
Advisor: Richard D. Schlichting

M.S in Computer Science **May 2001**
University of Arizona

B.E in Computer Science **June 1999**
Ramrao Adik Institute of Technology, Bombay University, Mumbai
Thesis : *CORBA Object Browser*

AWARDS AND HONORS

- Divisional Reconition Award - Microprocessor Technologies Lab, Intel, March 2009.
- Departmenal Recognition Award - Corporate Technology Group, Intel, October 2008.
- Certificate of Recognition for work on Future-Proof Data Parallel Algorithms and Software, Intel, November 2007.
- Divisional Recognition Award, Microprocessor Technologies Lab, Intel, November 2007.
- Certificate of Recognition for work on Runtime Environments for Tera-Scale Platforms, Intel, August 2007.
- Departmental Award of Excellence - Microprocessor Research Labs, Intel, August 2006.
- William C. Carter award for outstanding contribution based on dissertation research, IEEE/IFIP Dependable Systems and Networks, June 2005.
- IFIP/ACM Middleware 2001 Best Paper Award, June 2001
- Departmental Graduate Fellowship, Spring 2001

RESEARCH EXPERIENCE

Senior Research Scientist/Staff Software Engg. **Feb 2006 - Present**
Intel Corporation

Architected and implemented software prototypes of cutting edge technologies that were critical for enabling future multi-core and many-core platforms. While much of the work is confidential, it broadly spans new technologies ranging from language design and runtime optimization to memory models and micro-architectural support. High-level details include: designing and implementing new language features and architecture-support, implementing and optimizing managed runtimes with emphasis on new threading abstractions, scheduling mechanisms and memory models, as well as exploratory ideas for optimizing systems-software, etc.Notable highlights:

- Involved with 2 projects that went from early concept stage to alpha-product deliverable.
- Lead the developement of a production quality threading runtime for the Ct data-parallel language. Architected and implemented original software prototype, lead performance tuning efforts to make it competitive with and, in most cases, beat state of art
- Worked with (joint-pathfinding) compiler, O.S and application development teams.
- Collaborated with leading developers within Intel and external ISVs for software prototyping of demos that were shown at venues such as Intel Developer Forum(IDF) and Game Developers Conference(GDC)
- Experience with working-in and leading multi-national teams spanning across USA and China. Apart from engineering effort was also exposed to branding, placement and strategy aspects of product life-cycle.
- Mentored student interns and academic research projects with faculty at several top universities

Dept. of Computer Science, University of Arizona **Research Assistant** **Jan. 2000 - Dec 2005**

Member of the Cactus, Solar and Cassyopia research projects. Notable projects, in chronological order, include:

CQoS - Configurable Quality of Service
Developed a platform independent framework for configurable quality of service (*load balancing, fault tolerance, security and timeliness*). Ported the Cactus framework to Java RMI. Developed optimizations for server stubs. Developed a compiler for generating CQoS stubs. Evaluation on CORBA and Java RMI.

PLTO Binary Rewriting Toolkit
Developed several parts of the Pentium Link Time Optimizer (PLTO). Redesigned and rewrote low level infrastructure—Elf I/O routines, relocation mechanism ,assembler & disassembler; developed novel type-based disassembly algorithm; redesigned internal representations (e.g., CFG).

Optimizing Event Based Systems
Developed new compiler techniques for optimizing event-based systems. Developed a model for describing event-based execution, techniques for profiling event execution and optimizations targeting event and handler sequences. Experimental evaluation showed significant savings in a range of programs.

System Call Clustering
Developed a holisitic optimization approach that focuses on improving a program's entire system call behavior rather than reducing the cost of individual calls. Developed *multicall* mechanism using Linux kernel modules (x86 & StrongARM). Implemented *clustering* as a compiler optimization using PLTO.

System Security and Intrusion Tolerance
Developed Authenticated System Calls(ASC)—a new approach to system call monitoring that combines fine-grain sandboxing with policy-based expressiveness. Developed compiler-based techniques to automatically generate security policies through static analysis and transform application binaries to use ASC.

Automatic Kernel Customization
Developed *Charon*, a new binary rewriting framework targeted at transforming operating system kernel binaries. Currently exploring the use of Charon to automatically customize OS kernels for embedded devices by reducing the memory footprint and specializing for a given set of applications.

iPlanet Application Server, Sun Microsystems, Santa Clara **Intern** **May 2000 - Sept. 2000**

Worked on performance optimizations and redesign of connection path for iPlanet Application Server (iAS) v7.0. Achieved performance improvement in the ORB-Portable Object Adapter.

Dept. of Computer Engineering, University of Arizona **Research Assistant** **Aug. 1999 - Dec. 2000**

ABCOM Information Systems, Mumbai, India **Intern, Researcher** **Oct. 1998 - May 1999**

PUBLICATIONS

Patents

- System and Method for Enforcing Application Security Policies Using Authenticated System Calls, US Patent Application Serial No. 11/321,479. 2006.
- Concurrent Management of Parallel Adaptive Programs, Filed 2007.
- Future Scheduling By Direct Representation of Possible Dependencies, Filed 2007.
- Method and Apparatus for Supporting Scalable Coherence On Many-Core Products Through Restricted Exposure, Filed 2007.
- Method and Apparatus for Exception Handling in a Concurrent Setting, Submitted 2008.

  Several others in submission.

Journal Papers

1. Anwar Ghuloum, Terry Smith, Gansha Wu, Xin Zhou, Jesse Fang, Peng Guo, Byoungro So, Mohan Rajagopalan, Yongjian Chen, Biao Chen, "Future-Proof Data Parallel Algorithms and Software on Intel Multi-Core Architecture", *Intel Technology Journal*, Vol. 11, Issue 4, November 2007.
2. Bratin Saha, Ali-Reza Adl-Tabatabai, Rick Hudson, Vijay Menon, Tatiana Shpeisman, Mohan Rajagopalan, Anwar Ghuloum, Eric Sprangle, Anwar Rohillah, Doug Carmean, "Runtime Environment for Tera-scale Platforms" *Intel Technology Journal*, Vol. 11, Issue 3, August 2007.
3. Mohan Rajagopalan, Matti A. Hiltunen, Trevor Jim, Richard D. Schlichting, "System Call Monitoring through Authenticated System Calls", *IEEE Transactions on Dependable and Secure Computing (TDSC)*, Vol. 3 No. 3, 2006. **[Special issue on outstanding papers from DSN 2005]**.
4. Jun He, Matti A. Hiltunen, Mohan Rajagopalan, and Richard D. Schlichting, "QoS Customization in Distributed Object Systems", *Software Practice and Experience*, Vol. 33, pages 295-320, 2003. **[Special Issue on Middleware]**

Conference Papers

1. Bratin Saha, Xiaocheng Zhou, Hu Chen, Ying Gao, Shoumeng Yan, Mohan Rajagopalan, Jesse Fang, Peinan Zhang, Ronny Ronen, Avi Mendelson, "Programming Model for a Heterogeneous x86 Platform", *Programming Language Design and Implementation (PLDI)*, to appear 2009.
2. Mohan Rajagopalan, Shoumeng Yan, Anwar Ghuloum, "Primitives for Composable, Forward-scalable, Optimizable Parallel Programming", *Intel Programming Systems Conference*, April 2008.
3. Tood Anderson, Neal Glew, Peng Guo, Brian Lewis, Wei Liu, Zhanglin Liu, Leaf Petersen, Mohan Rajagopalan, James Stichnoth, Gansha Wu, and Dan Zhang, "Pillar: A Parallel Implementation Language", *Proceedings of 20th International Workshop on Languages and Compilers for Parallel Computing (LCPC 2007)*, Urbana, Illinois, October 2007.
4. Mohan Rajagopalan, Brian T Lewis, and Todd Anderson, "Thread scheduling for multi-core platforms", *Proceedings of USENIX Workshop on Hot Topics in Operating Systems (HotOS 2007)*, San Diego, CA, May 2007.
5. Bratin Saha, Ali-Reza Adl-Tabatabai, Anwar Ghuloum, Mohan Rajagopalan, Richard L Hudson, Leaf Petersen, Vijay Menon, Brian Murphy, Tatiana Spheisman, Jesse Fang, Eric Sprangle, Anwar Rohillah, Doug Carmean, "Enabling Scalability and Performance in a Large Scale Chip Multiprocessor Environment", *Proceedings of Eurosys 2007*, Lisbon, Portugal, March 2007.

6. Jim Stichnoth, Todd Anderson, Neal Glew, Peng Guo, Brian Lewis, Wei Liu, Zhanglin Liu, Leaf Petersen,Mohan Rajagopalan, Gansha Wu, Dan Zhang ,"The Pillar Software Stack for Concurrent Languages", *Intel Programming Systems Conference*, February 2007.

7. Biao Chen, Yongjian Chen, Zhaohui Du, Anwar Ghuloum, Zhenying Liu, Byoungro So, Mohan Rajagopalan, Zhigang Wang, Xin Zhou ,"The Ct Language", *Intel Programming Systems Conference*, Santa Clara, CA, February 2007.

8. Biao Chen, Yongjian Chen, Zhaohui Du, Anwar Ghuloum, Zhenying Liu, Byoungro So, Mohan Rajagopalan, Zhigang Wang, Xin Zhou ,"A Ct Implementation", *Intel Programming Systems Conference*, Santa Clara, CA, February 2007.

9. Matthew Hammer, Umut Acar, Mohan Rajagopalan, Anwar Ghuloum, "A Proposal for Parallel Self-Adjusting Computation", *Declarative Aspects of Multi-core Programming (DAMP'07)*, Nice, France, January 2007.

10. Mohan Rajagopalan, Somu Perinayagam, He Haifeng, Gregory Andrews, Saumya Debray, "Binary Rewriting and Instrumentation of an Operating System Kernel", *Workshop on Binary Instrumentation and Analysis (WBIA'06)*, San Jose, CA, October 2006.

11. Somu Perinayagam, Mohan Rajagopalan, He Haifeng, Gregory Andrews, Saumya Debray, "Profile-Guided Specialization of an Operating System Kernel", *Workshop on Binary Instrumentation and Analysis (WBIA'06)*, San Jose, CA, October 2006.

12. Cullen M Linn, Mohan Rajagopalan, Scott Baker, Christian Collberg, Saumya K. Debray and John Hartman, "Protecting Against Unexpected System Calls", *Proceedings of the 14th USENIX Security Symposium (SECURITY'05)*, Baltimore, MD, August 2005.

13. Mohan Rajagopalan, Matti A. Hiltunen, Trevor Jim, Richard D. Schlichting, "Authenticated System Calls", *Proceedings of the IEEE International Symposium on Dependable Systems and Networks (DSN 2005)*, Yokohama, Japan, June 2005. **[William C. Carter award]**

14. Mohan Rajagopalan, Saumya K. Debray, Matti A. Hiltunen and Richard D. Schlichting, "CASSYOPIA: Compiler Assisted Systems Optimization", *Proceedings of USENIX Workshop on Hot Topics in Operating Systems (HotOS 2003)*, Kauaii, USA, May 2003.

15. Mohan Rajagopalan, Saumya K. Debray, Matti A. Hiltunen and Richard D. Schlichting, "Profile Directed Optimization of Event Based Programs", *Proceedings of ACM Programming Language Design and Implementation (PLDI 2002)*, Berlin, Germany, July 2002.

16. Jun He, Matti A. Hiltunen, Mohan Rajagopalan, and Richard D. Schlichting, "Providing QoS Customization in Distributed Object Systems", *Proceedings of the IFIP/ACM International Conference on Distributed Systems Platforms (Middleware 2001)*, Heidelberg, Germany, November 2001. **[Best Paper Award]**

Magazine Articles

1. Mohan Rajagopalan and Poornachandra G. Sarang, "CORBA Object Browser", Java Developers Journal, June 1999. **[Special Featured Article in JavaOne Issue]**

Technical Reports and Manuscripts

1. Misc. white-papers at Intel.

2. Mohan Rajagopalan, Shoumeng Yan, Anwar Ghuloum, "Primitives for Composable, Forward-Scalable, Optimizable Parallel Programming", *In submission*.

3. Mohan Rajagopalan, Matthew Hammer, Umut Acar, Anwar Ghuloum, "Parallel Self-Adjusting Computation", *In submission*.

4. Mohan Rajagopalan, Saumya K. Debray, Matti A. Hiltunen, Richard D. Schlichting, "System Call Clustering: An automated approach to system call optimization", submitted for review to ACM Transactions on Computer Systems (TOCS), 2005.

5. Mohan Rajagopalan, Saumya K. Debray, Matti A. Hiltunen, Richard D. Schlichting, "Automatic Operating System Specialization via Binary Rewriting", *Technical Report, TR05-03*, Department of Computer Science, University of Arizona, March 2005.

6. Mohan Rajagopalan, Scott Baker, Saumya K. Debray, Matti A. Hiltunen, Richard D. Schlichting, and John H Hartman, "System call signatures and hidden fingerprints", *Technical Report, TR04-15*, Department of Computer Science, University of Arizona, August 2004.

7. Mohan Rajagopalan, Saumya K. Debray, Matti A. Hiltunen and Richard D. Schlichting, "Reducing the Energy Cost of Application/OS Interactions", *Technical Report, TR03-19*, Department of Computer Science, University of Arizona, March 2003.

8. Mohan Rajagopalan, Saumya K. Debray, Matti A. Hiltunen and Richard D. Schlichting, "Profile Directed Optimization of Event Based Programs", *Technical Report, TR03-05*, Department of Computer Science, University of Arizona, May 2003. (Expanded and revised version of PLDI paper.)

Posters and Work-In-Progress Talks

1. Mohan Rajagopalan, Saumya K. Debray, Matti A. Hiltunen, Richard D. Schlichting, "CHARON : A Framework for Automatic Kernel Specialization", *USENIX Operating Systems Design and Implementation (OSDI 2004)*, San Francisco, CA, December 2004.

2. Mohan Rajagopalan, Saumya K. Debray, Matti A. Hiltunen, Richard D. Schlichting, "System Call Clustering: An Automated Approach to System Call Optimization", *ACM Symposium of Operating Systems Principles (SOSP 2003)* , Lake George, NY, October 2003.

PROFESSIONAL AFFILIATIONS AND SERVICES

- Member of Association for Computing Machinery (ACM), ACM SIGOPS, ACM SIGPLAN
- Invited talk at SIAM-PP'08. Ct: C for Throughput Computing, Channeling Nesl and Sisal through C++, March 2008.
- Member of program committee for:
  International Conference on Distributed Computing Systems (ICDCS): 2007
  Intel Programming Systems Conference (IPSC) : 2007, 2008
  Workshop on Compiler and Architecture Techniques for Reliability and Security (CATARS) : 2009
- Reviewer for journals :
  ACM Transactions on Embedded Systems(TECS)
  Software Practice and Experience(SP&E)
  IEEE Transactions on Dependable and Secure Computing(TDSC)
- Reviewer for conferences :
  Dependable Systems and Networks (DSN): 2009, 2008, 2007, 2005
  Programming Language Design and Implementation (PLDI): 2008, 2007, 2006
  Principles of Programming Languages (POPL): 2008
  Symposium on Operating Systems Principles (SOSP): 2003
  Intel Programming Systems Conference (IPSC): 2007
  International Conference on Distributed Computing Systems (ICDCS): 2007
  Languages, Tools and Compilers for Embedded Systems (LCTES): 2007
  Virtual Execution Environments (VEE): 2007
  European Conference on Object Oriented Programming (ECOOP): 2009
  Symposium on Parallel Algorithms and Architectures (SPAA): 2009
- Session summarizer for USENIX Security Symposium (Security 2005)
- Session scribe for USENIX Operating Systems Design and Implementation (OSDI 2004)

- Member of service committees, Dept. of Computer Science, University of Arizona - Admissions (1999-2000), Research Computing (2001-2002), Curriculum (2002), Space Planning Committee (2004)
- Organized OASIS (Arizona Students in Systems) systems seminar in Department of Computer Science, University of Arizona, from Aug. 2001 - May 2002
- Conducted Graduate Assistants and Teaching Orientation (GATO 2001) sessions as a part of GPSC Graduate Orientation, University of Arizona, Aug. 2001

REFERENCES

Available upon request