

# Sriraman Tallam

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## RESEARCH INTERESTS

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Dynamic program analysis for **Tracing, Debugging, and Fault-Avoidance** in Multi-threaded Applications; **Program Profiling; Software Testing**; Optimizations for power and energy in **Embedded Systems**.

## EDUCATION

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<b>Ph.D. in Computer Science</b> The University of Arizona Thesis : Dynamic techniques for Fault Location and Avoidance in Multi-threaded Applications. Advisor : Prof. Rajiv Gupta	<b>Fall 2007</b> (expected)
<b>M.S. in Computer Science</b> The University of Arizona	<b>May 2003</b>
<b>M.C.A. (Master of Computer Applications)</b> Anna University	<b>May 2000</b>
<b>B.Sc. (Bachelor of Science) in Physics</b> University of Madras	<b>March 1997</b>

## AWARDS

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Graduate Student Research Award, Dept. of Computer Science, Univ. of Arizona, 2007.

## INDUSTRY EXPERIENCE

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<b>Software Engineer</b>	<b>Infosys Technologies Limited</b> Mangalore, India	<b>Jul. 2000 - Jun. 2001</b>
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## RESEARCH EXPERIENCE

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<b>Research Intern</b> <b>Mentor : Kshitij A. Doshi</b> <i>Platform Centric Integrated Performance Characterization</i> Developed methodologies to integrate platform events and processor events for performance characterization of industrial server workloads. This resulted in our team being the first within Intel to use platform events for performance monitoring.	<b>Intel Corporation</b> <b>Software Solutions Group</b>	<b>Summer 2006</b>
<b>Research Intern</b> <b>Manager : Hoi Vo</b>	<b>Microsoft Research</b> <b>Programmer Productivity Research Center</b>	<b>Summer 2004</b>
<b>Research Assistant</b> <b>Advisor : Rajiv Gupta</b>	<b>Dept. of Computer Science</b> <b>Univ. of Arizona</b>	<b>Fall 2002 - present</b>

*Scalable Collection and Storage of Program Traces* [TACO,PACT,ISSTA,FSE,CGO]  
I have developed techniques for efficiently collecting and storing the dynamic information (execution trace) from program executions involving one or more threads. These execution traces

are widely used in debugging and can be in of the order of gigabytes even for a few seconds of execution. I have developed a representation to enable the compact storage of these traces on disk. I have also developed techniques to enable the tracing of programs that run forever, which is infeasible for conventional trace collection techniques. I have also developed a technique to enable efficient profiling of those program paths which cross loop back-edges and procedure boundaries.

*Software Debugging, Testing and Fault-Avoidance* [PLDI,PASTE,TR-1]

I have contributed to the development of a technique to identify errors in a program that manifest due to omitting the execution of some statements. This is challenging using dynamic analysis because the omitted statements do not generate any dynamic information. I have contributed to the implementation of reverse breakpoints in *Microsoft Visual Studio cordbg* debugger. It is being achieved by enabling support for programs to step backwards during execution. In Software Testing, I have developed a very efficient heuristic for the test-suite minimization problem. I have developed a techniques to enable on-line recovery of faults caused by the execution environment in applications by perturbing the original execution. I have also developed techniques to prevent this fault from occurring more than once.

*Embedded Systems* [POPL,JavaPDC]

I have developed a register allocation algorithm that is aware of bitwidths of program variables and is capable of packing multiple subword variables into a single register. This research was targeted towards embedded processors that have instruction sets supporting referencing of bit sections within registers. I have developed a program partitioning technique to save energy on an embedded device when it is possible to execute parts of a program remotely on a server through wireless communication.

## JOURNAL PUBLICATIONS

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- [1] TACO            **S.Tallam** and R. Gupta, "Unified Control Flow and Dependence Traces," *ACM Transactions on Architecture and Code Optimization*, 30 pages, to appear.

## CONFERENCE PUBLICATIONS

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- [1] ISSTA            **S. Tallam**, C. Tian, X. Zhang, and R. Gupta, "Enabling Tracing of Long-Running Multithreaded Programs via Dynamic Execution Reduction," *International Symposium on Software Testing and Analysis*, London, UK, July 2007. Acceptance Rate : **22%** (22/101).
- [2] PLDI             X. Zhang, **S.Tallam**, N.Gupta, and R. Gupta, "Towards Locating Execution Omission Errors," *ACM SIGPLAN Conference on Programming Language Design and Implementation*, San Diego, June 2007. Acceptance Rate : **25%** (45/178).
- [3] FSE              X. Zhang, **S.Tallam**, and R. Gupta, "Dynamic Slicing Long Running Programs through Execution Fast Forwarding," *14th ACM SIGSOFT Symposium on Foundations of Software Engineering*, pages 81-91, Portland, Oregon, November 2006. Acceptance Rate : **20%** (25/125).
- [4] PACT             **S.Tallam**, R. Gupta, and X. Zhang, "Extended Whole Program Paths," *International Conference on Parallel Architectures and Compilation Techniques*, pages 17-26, Saint Louis, Missouri, September 2005. Acceptance Rate : **25%** (30/119).
- [5] CGO              **S.Tallam**, X. Zhang, and R. Gupta, "Extending Path Profiling across Loop Backedges and Procedure Boundaries," *Second Annual IEEE/ACM International Symposium on Code Generation and Optimization*, pages 251-262, San Jose, CA, March 2004. Acceptance Rate : **32%** (25/79).
- [6] POPL            **S.Tallam** and R. Gupta, "Bitwidth Aware Global Register Allocation," *30th Annual ACM SIGPLAN-SIGACT Symposium on Principles of Programming Languages*, pages 85-96, New Orleans, LA, January 2003. Acceptance Rate : **19%** (24/126).
- [7] TR-1             **S. Tallam**, C. Tian, X. Zhang, and R. Gupta, "Perturbing Program Execution For Avoiding Environmental Faults," *In Submission*.

## WORKSHOP PUBLICATIONS

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- [1] PASTE            **S.Tallam** and N. Gupta, "A Concept Analysis Inspired Greedy Algorithm for Test Suite Minimization," *ACM SIGPLAN-SIGSOFT Workshop on Program Analysis for Software Tools and Engineering*, Lisbon, Portugal, Sep. 2005. Acceptance Rate : **40%** (17/42).
- [2] JavaPDC        **S.Tallam** and R. Gupta, "Profile-Guided Java Program Partitioning for Power Aware Computing," *Sixth International Workshop on Java for Parallel and Distributed Computing*, Santa Fe, NM, April 2004.

## POSTERS

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- [1] PLDI            "Profile-Guided Java Program Partitioning for Power Aware Computing," *ACM SIGPLAN Conference on Programming Language Design and Implementation*, San Diego, CA, June 2003.

## RESEARCH TOOLS

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- **Valgrind** - Dynamic Binary Instrumentation Framework.
- **Microsoft Phoenix RDK** - Binary Instrumentation Tool.
- **LLVM Compiler Infrastructure**.
- **Jockey** - an user-space record/replay library.

## TEACHING EXPERIENCE

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- Fall 01,            TA    **University of Arizona**, Tucson,AZ  
CSc 344, *Foundations of Computing*, Teaching Assistant.
- Spring 02,        TA    **University of Arizona**, Tucson,AZ  
CSc 445, *Design and Analysis of Algorithms*, Teaching Assistant.
- Spring 07,        Grader **University of Arizona**, Tucson,AZ  
CSC 553, *Principles of Compilation*, giving lectures and grading.

## PROFESSIONAL ACTIVITIES

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- Member of Association for Computing Machinery (ACM).
- Volunteer at HPCA 2007, Phoenix, AZ.
- Reviewed papers for conferences and journals:

LCTES 07	ISCA 07	DATE 07	MICRO 06
Elsevier Journal 04	CASES 05	HiPEAC 05	MICRO 05
ICS 04	LCTES 04	HiPC 03	MICRO 03
ICS03	COLP 03	VPW 03	LARTES 02

## REFERENCES

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**Xiangyu Zhang** (Assistant Professor)  
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